REMARKS

Claim 1 was rejected over the patent to Nakata under Section 103 all by itself.

The viability, in general, of a single reference Section 103 rejection is doubtful. In order to make out a *prima facie* rejection there must be a teaching and a rationale to modify that teaching (which teaching, necessarily, does not meet the claim limitations), so that the teaching does meet the claim limitations. If that rationale is present in the reference, then a section 102 rejection would be appropriate. If the rationale is not present, a section 103 rejection could only be appropriate if the reference is combined with another teaching.

Here, we have two alternative arguments for why a single reference could make out a rejection. Firstly, it is suggested that the provision of a processor in the optical devices of the reference is inherent. However, to be inherent, the inherent feature must necessarily be used. There is no reason to believe that such a device could not be made wholly out of optical parts which do no processing whatsoever. This seems to be plainly the case with the elements recited in column 5 of the cited reference. They are plainly just a plurality of optical components.

Alternatively, the Examiner suggests that the claimed feature is well known. To the extent that the Examiner believes that it is well known to have a plurality of microprocessors coupled together by optical links within one device, he is respectfully requested to cite a reference.

Since a *prima facie* rejection is not made out, reconsideration is respectfully requested.

Concerning the objection to the drawings, it is noted that there is no requirement that the exact same words be used in the specification and claims. Clearly, what is shown in Figure 1 is a device. Therefore, Figure 1 supports the claim limitation.

Likewise, the arguments that there is a failure to comply with the written description requirement is noted, but there is no requirement that the same words be used in the specification and claims. It is suggested that the term "multiprocessor device" implies a device comprising a plurality of processors. It is suggested that a plurality of processors is not taught. A plurality of processors plainly is taught in Figure 1 and in the specification at page 3, lines 16-26. Moreover, multiprocessors are defined in page 3, lines 10-13, and the word multiprocessor system is used on page 3, line 16. Thus, it is plain that a multiprocessor system is taught and that multiprocessor systems are connected together on a printed circuit board or on the same die.

Further, it is suggested that there is no structure or circuit diagram provided to teach a person or ordinary skill in the art a plurality of processors. However, the plurality of processors are shown connected in Figure 1. How to connect them optically is shown in Figures 2, 3, 4, and 5. For example, in Figure 2, it is explained how to provide an optical interface between the electrical and optical units. In Figure 3, software is provided that analyzes the optical and electrical signals and coordinates between the different processors. In Figure 4, a structure is shown which handles the optical signals.

Thus, it is not clear what is believed to be missing. For example, a circuit diagram is unnecessary since this is basically a system which allows optical communications. Sufficient circuitry has been provided. There is no indication in the office action of what is believed to be missing.

Therefore, reconsideration is respectfully requested. It is noted, however, that on page 6, the Examiner suggests that it is extremely well known that optical transceiver comprise processors to process the signal. If this is so, this adds further doubt to the issue of the sufficiency of the disclosure.

Pending claim 21 calls for an article for a multiprocessor-based device including a second processor-based system and a third processor-based system to identify a light communication from a second processor-based system intended for the first processor-based system tuned to said wavelength and notify a third processor-based system that the first processor-based system is tuned to said wavelength.

Claim 21 is rejected as anticipated by Nakata. However, the application of Nakata clearly does not meet the limitations claimed since the claim calls for light communications between first and second processor-based systems and no such thing is shown in Nakata. In fact, the rejection does not even assert anything more than a node. Again, there is no reason to presume that the components are processor-based systems in Nakata.

Finally, there is no notifying a third processor-based system that the first processor-based system is tuned to a particular wavelength. In support of the rejection, column 5, lines 43-50, are cited. There is absolutely no suggestion within the cited material of notifying a third processor-based system that a first processor-based system is tuned to a wavelength. In fact, there is no notification between nodes in Nakata of what wavelength a particular node is tuned to.

Therefore, reconsideration of rejection of claim 21 is respectfully requested.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

Date: June 2, 2005

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation